AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (currently amended): An integrated semiconductor circuit device comprising a diode bridge circuit formed of a Schottky barrier diode and a periphery circuit formed of a MOS transistor which are formed on a single silicon substrate, wherein a Schottky barrier, which is a component of the Schottky barrier diode, is formed of a silicide layer, another silicide layer is formed on source/drain regions and a gate electrode, which are components of the MOS transistor, and both of the silicide layers are layers formed at the same time in self-alignment of the same materials ~~is made of a silicide layer~~.

Claim 2 (canceled)

Claim 3 (previously presented): A device according to claim 1, wherein the silicide layer is made of titanium silicide, tungsten silicide, cobalt silicide or platinum silicide.

Claim 4 (previously presented): A device according to claim 3, wherein the silicide layer shows a C54 phase.

Claim 5 (withdrawn): A process of manufacturing an integrated semiconductor circuit device comprising a diode bridge circuit formed of a Schottky barrier diode and a periphery circuit formed of a MOS transistor which are formed on a single silicon substrate, the process comprising the steps of:

exposing surfaces at desired positions in source/drain regions and a gate electrode of the MOS transistor, as well as in a region for forming a Schottky barrier of the Schottky barrier diode;

converting the exposed surfaces to amorphous;

forming metal layers capable of reacting to be silicide on the exposed surfaces;

subjecting the exposed surfaces and the metal layers to a thermal treatment for silicidation to form silicide layers; and

conducting a thermal treatment for reducing a resistance of the silicide layers.

Claim 6 (withdrawn): A process according to claim 5, wherein the thermal treatments for the silicidation and the reduction of the resistance of the silicide layers are carried out by Rapid Thermal Anneal.

Claim 7 (withdrawn): A process according to claim 5, wherein the silicide layers are formed in self-alignment.

Claim 8 (withdrawn): A process according to claim 5, wherein the silicide layers are made of titanium silicide and the titanium silicide layers are changed in phase from C49 to C54 at the thermal treatment for reducing the resistance thereof.

Claim 9 (previously presented): An IC module including an integrated semiconductor circuit device according to claim 1.

Claim 10 (previously presented): An IC card including an IC module according to claim 9.